Docket No.: JCLA8533 Application No.: 10/055,568

AMENTMENTS

Amendments to the claim

Claims 1-142 (canceled)

143. (new) A chip package structure comprising:

a substrate comprising silicon;

only one die mounted to said substrate, said die having an active surface, an internal circuitry and a plurality of active devices, said active surface including multiple pads electrically connected to said active devices through said internal circuitry, said substrate having a surface not covered by said die; and

at least one patterned line extending over said active surface of said die and over said surface of said substrate, said patterned line electrically connected to one of said pads, said patterned line constructed from at least a patterned circuit layer.

144. (new) The structure in claim 143, wherein a thickness of said patterned line is greater than that of a trace of said internal circuitry.

145. (new) The structure in claim 143, wherein a width of said patterned line is greater than that of a trace of said internal circuitry.

146. (new) The structure in claim 143, further comprising a power bus positioned over said active surface of said die.

147. (new) The structure in claim 143, further comprising a ground bus positioned over said active surface.

148. (new) The structure in claim 143, further comprising a dielectric layer positioned over said active surface of said die and said surface of said substrate, said patterned line positioned over said dielectric layer, said dielectric layer having multiple via holes, said patterned line electrically connected to said pads through said via holes.

149. (new) The structure in claim 148, wherein a material of said dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

150. (new) The structure in claim 143, further comprising a dielectric layer positioned over said patterned line.

151. (new) The structure in claim 150, wherein a material of said dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

152. (new) The structure in claim 143, further comprising at least one passive device positioned over said substrate and electrically connected to said die.

153. (new) The structure in claim 152, wherein said passive device comprises a resistor.

154. (new) The structure in claim 152, wherein said passive device comprises an inductor.

155. (new) The structure in claim 152, wherein said passive device comprises a capacitor.

156. (new) The structure in claim 143, wherein said substrate further comprises a cavity accommodating said die.

157. (new) The structure in claim 156, wherein said active surface of said die is coplanar with said surface of said substrate.

158. (new) The structure in claim 143, wherein said substrate comprises a silicon layer and a heat conducting layer, said silicon layer positioned over said heat conducting layer, said surface of said substrate provided by an upper surface of said silicon layer, said silicon layer having an opening exposing said heat conducting layer, said die positioned in said opening and over said heat conducting layer.

159. (new) The structure in claim 158, wherein said upper surface of said silicon layer is coplanar with said active surface of said die.

160. (new) The structure in claim 143, further comprising a polymer layer positioned over said surface of said substrate, said die having a side wall enclosed by said polymer layer.

161. (new) The structure in claim 160, wherein said polymer layer has an upper surface coplanar with said active surface of said die.

162. (new) The structure in claim 160, wherein a material of said polymer layer is selected from a group consisting of epoxy.

163. (new) The structure in claim 143, further comprising multiple solder balls positioned over said surface of said substrate.

164. (new) The structure in claim 143, wherein said substrate is made of bulk silicon.

165. (new) The structure in claim 143, further comprising at least one interconnection patterned line positioned over said active surface, said interconnection patterned line constructed from at least a patterned circuit layer, wherein a signal is suited to be transmitted from one of said active devices to other of said active devices through said internal circuitry and said interconnection patterned line.

166. (new) The structure in claim 165, wherein a thickness of said interconnection patterned line is greater than that of a trace of said internal circuitry.

167. (new) The structure in claim 165, wherein a width of said interconnection patterned line is greater than that of a trace of said internal circuitry.